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# RN-8191

## B. E. II (Sem. IV) (Computer) Examination

### May / June – 2010

## Microprocessor & Interfacing

Time : 3 Hours] [Total Marks : 100

**Instruction :**

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
**Fillup strictly the details of ☛ signs on your answer book.**

Name of the Examination :

☛ **B. E. 2 (Sem. 4) (Computer)**

Name of the Subject :

☛ **Microprocessor & Interfacing)**

☛ Subject Code No. : **8 1 9 1** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

### Section 1

Q. 1 A Answer the following: 10

1 Define Machine Cycle.

2 What is the direction of address bus?
a) Uni – directional into microprocessors
b) Uni – directional out of microprocessors
c) Bi – directional

3 Give advantage of having registers of 8085 built inside the microprocessor and not in memory.

4 How does a microprocessor differentiate between data and instruction code?

5 The largest number that can appear on an 8085 microprocessor data bus is _____H.

6 Write a single logical instruction which clears accumulator.

7 The Instructions used for data transfer in I\o mapped I\O are
a) IN, OUT b) IN, LDA add
c) STA add d) None of the above

8 Number of Address lines required to interface 1KB of memory are
a) 10 b)11 c) 12 d) 13

9 Shadow Address will exist in
a) absolute decoding b) partial decoding

10 To operate 8085 microprocessor at 1.1 MHZ, the crystal should have frequency of ___ MHZ.

B Explain function of following 8085 pins: 3
ALE, HOLD, INTR

C Specify addressing modes and Explain the following instructions: 4
1. LDAX 2. POP PSW

D Mention machine cycles and T-states for the following instructions: 3
1. MOV M, R 2. XCHG 3. MVI A, 08h



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Q.2 A Two machine codes 3EH and 32H are stored in memory locations 2000h and 2001H, respectively. The first machine code represents the opcode to load a data byte in the accumulator, and the second code represents the data byte to be loaded in the accumulator. Illustrate the bus timings as these machine codes are executed (i.e. MVI A, 32H). 7

B Write an 8085 program that simulates the following 'C' module: 8

```
for(i = 0;i<=5;i++)
{
A[i]=B[i]+2;
}
```

Note : A and B are arrays consisting of 8-bit data elements.

**OR**

B Write an 8085 main program and a conversion subroutine (BCDBIN) to convert the BCD number into its equivalent binary number. 8

Q.3 A Interface 10

- 8K × 8 EPROM
- 16 K × 8 RAM using 8K × 8 chips

To 8085.Draw the neat diagram showing the interface scheme and clearly explain the memory map for both the devices. Make necessary assumptions and explain through diagram.

B What is BUS? Draw and explain 8085 Bus structure. 5

**OR**

B Draw functional block diagram of 8085 architecture. 5

# SECTION - II

| | | |
|---|---|---|
| Q.4 (a) | Answer the followings.(Any Ten)<br>(1) Explain Handshake signals.<br>(2) Explain instruction EI.<br>(3) Explain BSR mode of 8255A.<br>(4) RST instruction is 1 byte call instruction.- State True or False.<br>(5) Explain HOLD signal?<br>(6) A/D converters can serve as input devices to microprocessor based system. – State True or False.<br>(7) List the four major sections of 8279.<br>(8) What is the use of FIFO RAM in 8279?<br>(9) What is A/D converter?<br>(10) What do you mean by simplex transmission?<br>(11) TRAP has highest priority.- State True or False.<br>(12) Interrupt Acknowledgement is active low signal.- State True or False. | (10) |
| Q.4 (b) | Answer the following (Any Two)<br>(1) Explain different key debouncing techniques.<br>(2) What is synchronous and asynchronous communication? Briefly discuss.<br>(3) Explain SIM and RIM instructions with there use. | (10) |
| Q.5 (a) | Draw and explain 8255 programmable peripheral interface IC. | (8) |
| Q.5 (b) | Describe the functioning of 8259 programmable interrupt controller with the help of block diagram.<br>OR | (8) |

| | | |
|---|---|---|
| Q.5 (b) | Draw and explain 8251 programmable communication interface. | (8) |
| Q.6 (a) | Explain 8254 Programmable Interval Timer with the help of block diagram. | (10) |
| Q.6 (b) | Explain interrupts and its types.<br>OR | (4) |
| Q.6 (b) | Explain pending interrupts and DI . | (4) |